REMARKS

This response is intended as a full and complete response to the Office Action dated June 17, 2005. In view of the amendments and the following discussion, the Applicants believe that all claims are in allowable form.

I. OBJECTIONS

a) SPECIFICATION

The Examiner objected to the specification because title of the abstract did not match the title in the specification. In response, the applicants have amended the title of the abstract accordingly. As such, the applicants respectfully request that the objection be withdrawn.

b) CLAIMS

Claims 4, 8, 18, 22, and 31

The Examiner has objected to claims 4, 8, 18, and 31 due to improper numbering. In response, the applicants have amended claims accordingly. As such, the applicants respectfully request that the objection be withdrawn.

Claims 29 and 34

The Examiner has objected to claims 29 and 34 as containing limitations expressed in unclear language. The Examiner suggests that claims 28 and 29 are synonymous because the Examiner considers the terms "host workstation" and "testbench process" as being synonymous. The Applicants respectfully disagree.

The testbench process is a process that is executed by the host workstation. As recited in Claim 27, when a service request occurs a signal is sent to the testbench process. Since the testbench process is executed by the host workstation, the signal can be recited as being applied to either the host workstation or a particular process executed by the workstation. The use of the host workstation to service the signal (claim 29) is a broader recitation than the recitation of using the specific testbench process to service the signal (claim 29). Since the scope of these claims is

substantially different, claims 28 and 29 should not be considered synonymous. Furthermore, the applicants believe the recitation of the "testbench process" in claim 29 is clear as written and finds antecedent basis in the third line of claim 27. A similar argument can be made for claim 34. As such, the applicants respectfully request that the objection to claims 29 and 34 be withdrawn.

II. CLAIM REJECTIONS

A. 35 U.S.C. §102(e) Claims 1-11, 13-15, 17-30, 32-34, and 36

Claims 1-11, 13-15, 17-30, 32-34, and 36 stand rejected as being anticipated by United States Patent No. 5,838,948 issued Nov. 17, 1998 to *Bunza* (hereinafter referred to as "*BU'948*").

BU'948 teaches a system and method for simulation of target electronics ("user design") using a host workstation operating a process emulator and a hardware simulator coupled using a software kernel. A part of the target electronics is modeled using the process emulator ("reprogrammable logic"), while the hardware simulator and kernel are both software components. The hardware simulator contains a process model shell emulating the actual pin connections of a target microprocessor (Fig. 6; col. 10, lines 20-26, 62-65).

At column 5, lines 62-67, *BU'948* states that "most hardware simulators allow multiple levels of modeling abstraction from a switch or transistor level model to a high level behavioral model." *BU'948* does not discuss further how the hardware simulator actually simulates such levels of abstraction. Furthermore, at column 5, lines 46-47, *BU'948* specifically states that the "hardware simulator" is a "software program". In contrast to a hardware simulator, *BU'948* then describes (at column 9, lines 8-20) an invention that uses a "hardware emulator" formed of reconfigurable circuitry, e.g., an FPGA. *BU'948* goes on to state, at column 9, lines 49-52, that the use of "behavioral or high-level design representations, typical of early stages of design, are precluded by the use of hardware emulators." Nowhere does *BU'948* discuss the use of high-level design representations within hardware emulators. *BU'948* is devoid of any further

disclosure of modeling within the reprogrammable logic (i.e., a hardware emulator) a behavior level function.

In contrast, the applicants' claim 1 specifically recites "a reprogrammable logic element for modeling a hardware model of the portion of the user design that includes a behavior level function". *BU'948* is devoid of any such teaching. Consequently, *BU'948* is also devoid of any teaching of "a testbench call back process for responding to the behavior level function in the reprogrammable logic element", as also recited in applicants' claim 1.

Independent claims 13, 27, and 32 also recite similar subject matter as recited in claim 1.

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 221 USPQ 481, 485 (Fed. Cir. 1984) (emphasis added). Since *BU'948* lacks any disclosure of a behavior level function being modeled in a reprogrammable logic element, the applicants contend that claims 1, 13, 27, and 32 are patentable over *BU'948* and, as such, fully satisfy the requirements of 35 U.S.C. §102 and are patentable thereunder.

Furthermore, claims 2-11, 14-15, 17-20, 22-23, 25-26, 28-30, 33-34, and 36 depend, either directly or indirectly, from claims 1, 13, 27, and 32 and recite additional features therefor. Thus, the applicants submit that independent claims 1, 13, 27, and 32 and claims 2-11, 14-15, 17-20, 22-23, 25-26, 28-30, 33-34, and 36 depending therefrom are patentable over *BU'948*. Accordingly, the Applicants respectfully request the rejection be withdrawn.

B. 35 U.S.C. §103(a) Claims 4, 16, 31, and 35

Claims 4, 16, 31, and 35 stand rejected as being unpatentable over *BU'948* in view of IEEE Std 1364-1995 "IEEE Standard Hardware Description Language based on the Verilog® Hardware Description Language" (hereinafter referred to as "*IEEE1364*").

Independent claims 1, 13, 27, and 32, as discussed above, recite a reprogrammable logic element that models a behavior function (or behavioral portion)

of a user design. *BU'948* does not teach or suggest modeling a behavior function or behavioral portion of a user design in a reprogrammable logic element. In fact, *BU'948* suggests that using reprogrammable logic precludes high-level modeling needed for behavioral function modeling.

IEEE1364 teaches conditional expression for state dependent paths, but is devoid of any teaching or suggestion of using a reprogrammable logic element to model a behavioral function of a user design. Nor is there any disclosure of using a testbench call back process that responds to the behavioral function. Since the same elements are lacking from both *BU'948 and IEEE1364*, no permissible combination of these references teaches or suggests the applicants' invention as recited in independent claims, 1, 13, 27, and 32.

Claims 4, 16, 31, and 35 depend, either directly or indirectly, from claims 1, 13, 27, and 32 and recite additional features therefor. Since a combination of *BU'948* and *IEEE1364* would not produce applicants' invention as recited in claims 1, 13, 27, and 32, dependent claims 4, 16, 31, and 35 are also not obvious and are allowable.

Thus, the applicants submit that claims 4, 16, 31, and 35 are patentable over *BU'948* in view of *IEEE1364*. Accordingly, the applicants respectfully request the rejection be withdrawn.

C. 35 U.S.C. §103(a) Claims 12 and 37

Claims 12 and 37 stand rejected as being unpatentable over *BU'948* in view of an article "A 145MHz User-Programmable Gate Array" by Eduardo do Valle Simoes et al. (IEEE Transactions on Computers, 1995, pp. 226-232, hereinafter referred to as *"ED1995"*).

Independent claims 1 and 32, as discussed above, recite a reprogrammable logic element that models a behavior function or behavioral portion of a user design. *BU'948* does not teach or suggest modeling a behavioral function or portion in a reprogrammable logic element. In fact, *BU'948* suggests that using reprogrammable logic precludes high-level modeling needed for behavioral function modeling.

ED1995 teaches conditional expression for state dependent paths, but is devoid of any teaching or suggestion of using a reprogrammable logic element to model a behavioral function of a user design. Nor is there any disclosure of using a testbench call back process that responds to the behavioral function. Since the same elements are lacking from both *BU'948 and ED1995*, no permissible combination of these references teaches or suggests the applicants' invention as recited in independent claims 1and 32.

Claims 12 and 37 depend, either directly or indirectly, from claims 1 and 32 and recite additional features therefor. Since the combination of *BU'948* and *ED1995* would not produce Applicants' invention as recited in claims 1 and 32, dependent claims 12 and 37 are also not obvious and are allowable.

Thus, the applicants submit that claims 12 and 37 are patentable over *BU'948* in view of *ED1995*. Accordingly, the applicants respectfully request the rejection be withdrawn.

CONCLUSION

Thus, the applicants submit that all claims now pending are in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issuance are earnestly solicited.

If, however, the Examiner believes that any unresolved issues still exist, it is requested that the Examiner telephone Mr. Raymond R. Moser, Jr. at (732) 935-7100 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

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Sept. 19, 2005
Date of signature

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